REMARKS/ARGUMENTS

After the foregoing Amendment, claims 1-18 are currently pending in this application. Claim 16 has been amended to more distinctly claim subject matter which the Applicants regard as a feature of the invention. Applicants submit that no new matter has been introduced into the application by the amendment.

Allowable Subject Matter

Applicants note with gratitude that claims 3-4, 7-9, and 17 contain allowable subject matter.

Claim Rejections - 35 USC § 102

Claims 12, and 15-16, stand rejected under 35 USC § 102(b) as being allegedly anticipated by *House* (US Patent No. 4,796,232). Applicants respectfully traverse this rejection.

The claims are directed to a memory controller connection to memory using a buffer. The memory controller and buffer are connected by a bidirectional data bus and a control interface, and the buffer is connected to a random-access memory bus for read and write operations. The buffer comprises data storage areas to buffer data between the controller and the memory. The buffer further comprises logic circuits to decode control commands from the controller, and the buffer and memory are also connected by a data access and control bus to control read and write operations from and to the memory.

One advantage of such an arrangement is that the controller and the buffer can be in one timing domain, and the buffer and memory can be in a separate timing domain. This can simplify system timing and increase realized bandwidth to memory, for example, where a fast

controller is used to control more than one slower logical memory bus. Another advantage is that reads and writes can be buffered to produce long sequences, thereby reducing the number of bus turns. Each time the bus driving direction is turned, bandwidth is lost since data cannot be transferred during this time, so fewer turns can result in higher realized bandwidth. In addition, in memory such as DRAM, bus turns can take longer than bus turns in a memory controller because DRAM strobes must be turned as well, increasing the turn window. Also, where different sets of DRAM share a common bus, the bus may have unutilized time between the reads from the different sets of DRAM, to avoid drive fight. These factors can combine to further reduce the bandwidth of the DRAM bus. The apparatus and methods as recited in the claims can improve memory bandwidth by reducing the number of bus turns.

In contrast to the present application, *House* discloses a dual port memory controller, operative to interface a pair of processors to a common bank of memory. A logic array provides arbitration between conflicting dual processor and memory refresh requests for memory access, and the memory is refreshed in a staggered fashion to minimize noise created during refresh and to maintain the availability of a portion of the memory for read/write operations at all times. Although *House* discloses a memory controller, buffers, and memory, their arrangement and operation are different than in the present claims. In *House*, the controller acts to arbitrate traffic between system memory and two processors A and B. When processor A wants to read the memory, the memory address it wants to read from is stored in address buffer **50**, and a request for memory access is issued by processor A to the controller. The controller resolves any conflicting requests for memory access, determines when to allow the memory to be read by processor A, and provides the appropriate control signals. The data in the buffered address is then retrieved from memory and passed through to processor A (*House* column 5 line 43 –

column 6 line 25). When processor A wants to write to memory, the memory address it wants to write to is stored in address buffer **50**, and the data it wants to write is stored in data buffer **60**, and a request for memory access is issued by processor A to the controller. The controller resolves any conflicting requests for memory access, determines when to allow the memory to be written by processor A, and provides the appropriate control signals. The buffered data is then written to the buffered memory address (*House* column 6 line 65 – column 7 lines 21). The controller similarly controls processor B's access to memory (*House* column 6 lines 53-64 for memory reads, and column 7 lines 22 – 35 for memory writes). As noted in *House* column 7 lines 60 – 64, "the basic function of gate array **10** [i.e., the controller] is to resolve the conflict which results from simultaneously (*sic*) requests to access memory **16** from the three possible sources of processor A, processor B and the refresh system."

It is well settled that a reference must teach every element or aspect of a claim in order to be considered prior art under 35 USC § 102(b).

The arrangement of elements in *House* is easily distinguished from the arrangement of elements in the claims, and in certain respects *House* is essentially the opposite of the claimed arrangement. In *House*, at least two processors are required, both accessing the same memory, and the controller coordinates the processors' access to the memory. Direct connections with buffers are provided to the processors and to the memory. *House* serves no function in a system having only a single processor, and *House* is not applicable with regard to a system having a plurality of independent memories.

In contrast, the method of claims 12 and 15-16 does not require at least two processors, but can be used effectively in a system having only a single processor. Direct connections with buffers are not provided to the processors. The method claimed is applicable with regard to a

system having a plurality of independent memories. In fact, whereas *House* operates to coordinate the access of two independent processors to a single memory, the method claimed can be used to coordinate the access of a single processor to two independent memories, a configuration which is essentially the opposite of what is disclosed in *House*.

Referring to claim 12, the examiner asserts that *House* discloses a method for data transfer between a memory controller and a system memory bus connected to a system memory. That is not correct. Rather, in *House*, the controller provides only control signaling. Data is not transferred between the controller and the memory, but only between the processors and the memory. The examiner also asserts that *House* interposes a buffer between the system memory bus and the memory controller. That is not correct. Rather, *House* interposes buffers between the system memory bus and each of two processors, but only control signals pass to and from the controller. The examiner also asserts that *House* transfers read and write memory data between the memory controller and the buffer during read and write operations. That is not correct. Rather, *House* teaches transferring read and write memory data between the buffers and the processors, but does not teach transferring read and write memory data between the memory controller and the buffers.

Because *House* does not teach all of the elements of claim 12, it does not anticipate claim 12 under 35 USC § 102(b), and claim 12 is allowable over *House*.

Claims 15-16 depend from claim 12, and without prejudice to their individual merits, are deemed allowable for at least the same reasons as claim 12. In addition, with reference to claim 16, *House* does not disclose fanning memory address information received in the buffer to more than one system memory bus, as does claim 16. For this reason also, claim 16 is deemed allowable over *House*.

Based on the arguments presented above, reconsideration and withdrawal of the 35 USC § 102(b) rejection of claims 12 and 15-16 are respectfully requested.

Claim Rejections - 35 USC § 103(a)

To establish a *prima facie* case for obviousness under 35 USC § 103(a), it must be shown that the asserted references, when read alone or in combination, teach all of the elements of the examined claims. In addition, a motivation to combine the references must be shown if more than one reference is being asserted.

Furthermore, the factual inquiries set forth in *Graham v. John Deere*, 383 U.S. 1 (1966), should be made to establish the background for determining obviousness under 35 USC § 103(a). Those inquiries are: determining the scope and contents of the prior art; ascertaining the differences between the prior art and the claims at issue; resolving the level of ordinary skill in the pertinent art; and considering objective evidence present in the application indicating obviousness or non-obviousness.

Claims 1, 5-6, 10-11 and 18 stand rejected under 35 USC § 103(a) as being allegedly unpatentable over *Platko* (U.S. Patent No. 6,363,444) in view of *House* (same as above). The rejection is traversed.

Platko discloses a processing system in which a master processor is coupled to a memory via a memory data bus. The master processor supplies an address and control signals to the memory, enabling the master processor to control the reading and writing of the memory at addressed locations. A slave processor, such as an encryption engine, has a data input/output bus connected directly to the memory data bus. The master processor supplies control signals to the slave processor to control the reading and writing of data to/from the slave processor via the

memory data bus. (*Platko* column 2 lines 17-29.) *Platko* discloses using such an arrangement in a network interface card (NIC), which operates to move packets between a network segment **14** and a host memory that is accessible via a PCI bus **12**. All packets either transmitted or received are buffered in SRAM **20**. (*Platko* column 4 lines 1-4).

Regarding claim 1, the examiner asserts *Platko* discloses "said buffer being connected to a random-access memory bus for read and write operations", citing Figure 1 items 20, 22, and 46. That is incorrect. As is clear from Figure 1, SRAM **20** (the buffer) is connected only to memory controller **46** via bidirectional bus **22**. There is no connection between the buffer and a random access memory bus, as in claim 1.

The examiner admits that *Platko* fails to disclose the remaining elements of claim 1, and asserts that *House* "helps" disclose those elements. It is respectfully submitted that a claim element is either disclosed or it is not. Applicants do not understand whether a claim element that requires "help" to be disclosed is disclosed in the base reference, or in the added reference, or not disclosed in either reference, and if not disclosed, whether it was suggested in one reference or the other, or neither disclosed nor suggested in either reference. MPEP 2142 states that "the examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness." For the examiner to make out a *prima facie* case of obviousness under 35 USC § 103, "the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (MPEP 2142 Legal Concept of Prima Facie Obviousness.) Applicants respectfully contend that by citing references that "help" disclose a claim element, the

examiner does not meet the burden of establishing a *prima facie* case of obviousness, because the element was neither disclosed nor suggested as required.

Nevertheless, without prejudice or disclaimer, in order to advance prosecution of the present application, applicants will hereinafter present arguments as though the examiner were asserting that the "helped" elements were actually disclosed. The first such element recites "said buffer comprising data storage areas to buffer data between the memory controller and system memory." As has been described hereinbefore, in *House*, data is not transferred between the controller and the memory, but only between the processors and the memory. Thus, *House* does not disclose buffering data between the memory controller and system memory, but only between the processors and the memory.

Furthermore, there is no teaching or suggestion in either *Platko* or *House* that their features be combined. And since neither reference discloses buffering data between the memory controller and system memory, there is no possible combination of the references that would result in such a feature.

In addition, the examiner asserts it would have been obvious to combine *Platko* with *House* to "aid in the control of the transfer of information to and from memory." That motivation is unlikely. *Platko* is directed to a processing system in which a slave co-processor is supported without requiring a separate interface on a master processor, thereby achieving high system performance while keeping device pin counts low and reducing device cost and complexity (*Platko* column 2 lines 11-16). *House* is directed to interfacing a pair of processors to a common memory and providing arbitration between conflicting processor requests for memory access (*House*, abstract). Neither reference is directed to or concerned with "the control of the transfer of information to and from memory" in the generic sense suggested by the

examiner. It is respectfully submitted that it is only with impermissible hindsight that the features of the cited references would be combined in the manner suggested by the examiner.

Based on the arguments presented above, the 35 USC § 103(a) rejection of claim 1 is not supported, and claim 1 is allowable over the cited prior art.

Claims 5-6 and 10-11 depend from claim 1 and, without prejudice to their individual merits, are deemed allowable over the cited references for at least the same reasons as claim 1.

Claim 18 is analogous to claim 1, and the arguments presented above with regard to claim 1 are also applicable with regard to claim 18. Claim 18 is therefore deemed allowable for at least the same reasons as claim 1.

Claims 13-14 stand rejected under 35 USC § 103(a) as being allegedly unpatentable over *House* (same as above) in view of *Fortuna* (U.S. Patent No. 6,546,464). The rejection is traversed.

Claims 13-14 depend from claim 12, and it is noted that *Fortuna* is relied on only for the additional features of claims 13-14. Therefore, without prejudice to their individual merits, claims 13-14 are deemed allowable over the cited references for at least the same reasons as claim 12 is allowable.

In addition, with reference to claim 13, the examiner asserts that *Fortuna* "helps" disclose a "processor module" including system memory, direct memory access device(s), memory controller, processor(s) with associated cache(s) and tag buffer. The arguments presented above regarding whether a reference that "helps" disclose a claim element can be adequate to meet the examiner's burden of making a *prima facie* case of obviousness under 35 USC § 103 apply to this claim, as well as to other claims for which the examiner cites references that "help" disclose

claim limitations, and applicants do not believe a *prima facie* case has been made with regard to those claims. Nevertheless, without prejudice or disclaimer, in order to advance prosecution, applicant will present arguments as though the examiner were asserting that the "helped" elements were actually disclosed.

The examiner appears to have cited *Fortuna* for the element which claim 13 adds to claim 12, "interposing a second buffer between the controller and system memory serving as a tag buffer," citing *Fortuna* column 4 lines 51-55. However, *Fortuna* at the cited location discloses a tag buffer (and the other components recited by the examiner, not all of which are found in claim 13) "communicatively coupled as depicted [in Figure 1]." Figure 1 depicts the tag buffer **112** with processor(s) **114**, or arguably interposed between the processor(s) **114** and system memory **108**. However, it is impossible to interpret Figure 1 as interposing the tag buffer between memory controller **118** and system memory **108**, because the communicative coupling between memory controller **118** and system memory **108** depicted in Figure 1 is completely separate and distinct from the communicative coupling between system memory **108** and tag buffer **112**. Therefore, "a second buffer between the controller and system memory serving as a tag buffer" is not disclosed or suggested by the cited references in any possible combination, therefore claim 13 is deemed allowable over the cited references.

In addition, with reference to claim 14, claim 14 depends from claim 13, and it is noted that *Fortuna* is relied on only for the additional features of claim 14. Therefore, without prejudice to its individual merits, claim 14 is deemed allowable over the cited references for at least the same reasons as claim 13.

Furthermore, claim 14 recites "updating memory tag information through a tag interface control bus between the memory controller and the tag buffer." Neither *House* nor *Fortuna*,

either alone or in any possible combination, disclose or suggest a tag interface control bus between the memory controller and the tag buffer. For this reason also, claim 14 is deemed allowable over the cited prior art.

Also, the examiner does not suggest any motivation for combining the features of *House* and *Fortuna* to arrive at claim 14, as required by and explained in MPEP 2142. Therefore, the examiner has failed to make out a *prima facie* case of obviousness. And, neither *House* nor *Fortuna* suggests combining their features in the manner suggested by the examiner. Applicant respectfully contends it is only with impermissible hindsight in view of the present application that the examiner has asserted the suggested combination is obvious. For this reason also, claim 14 is deemed allowable over the cited prior art.

Claim 2 stands rejected under 35 USC § 103(a) as being allegedly unpatentable over *Platko* (same as above) in view of *House* (same as above) and further in view of *Fortuna* (same as above). The rejection is traversed.

Claim 2 depends from claim 1, and it is noted that *Fortuna* is relied on only for the additional features of claim 2. Therefore, without prejudice to its individual merits, claim 2 is deemed allowable over the cited references for at least the same reasons as claim 1.

In addition, the examiner asserts that *Fortuna* "helps" disclose a "processor module" including system memory, direct memory access device(s), memory controller, processor(s) with associated cache(s) and tag buffer. The arguments presented above regarding whether a reference that "helps" disclose a claim element can be adequate to meet the examiner's burden of making a *prima facie* case of obviousness under 35 USC § 103 also apply to this claim, and applicants do not believe a *prima facie* case has been made with regard to claim 2.

Furthermore, the examiner cites *Fortuna* column 4 lines 51-55 and Figure 1 as "helping" to disclose the features recited in claim 2, but applicants are unable to locate the recited features at the cited location, and do not believe they can be found at the cited location or elsewhere in the cited references.

Moreover, none of the cited references suggests combining their features in the manner suggested by the examiner. Applicant respectfully contends it is only with impermissible hindsight that the examiner has combined their features in the manner suggested.

For these reasons, claim 2 is deemed allowable over the cited prior art of record.

In view of the arguments presented above, withdrawal of the 35 USC § 103(a) rejection of claims 1-2, 5-6, 10-11, 13-14, and 18 is respectfully requested.

Conclusion

In view of the foregoing amendment and remarks, Applicants respectfully submit that the present application, including claims 1 – 18, is in condition for allowance and a notice of allowance is respectfully requested.

If the Examiner believes that any additional minor formal matters need to be addressed in order to place this application in condition for allowance, or that a telephone interview will help to materially advance the prosecution of this application, the Examiner is invited to contact the undersigned by telephone at the Examiner's convenience.

Respectfully submitted,

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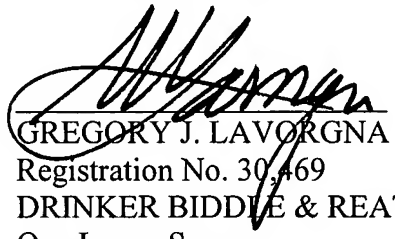
BY: 

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